In the Claims

CLAIMS

Claims 1-33 (Canceled).

34. (Previously presented) A transistor assembly comprising:

a plurality of active areas having widths defined by shallow trench isolation regions, wherein the widths of the active areas are no greater than about one micron and at least some of the widths are different; and

gate lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another.

35. (Original) The transistor assembly of claim 34, wherein the threshold voltages of at least some of the individual transistors are less than one volt.

36. (Original) The transistor assembly of claim 34, wherein individual transistors having active areas with the smaller widths have threshold voltages which are smaller than other individual transistors having active areas with larger widths.

37. (Previously presented) The transistor assembly of claim 34, wherein one of the individual transistors comprises a portion of precharge circuitry for dynamic random access memory circuitry.

38. (Previously presented) The transistor assembly of claim 34, wherein one of the individual transistors comprises a pass transistor.

39. (Previously presented) The transistor assembly of claim 34, wherein one of the individual transistors comprises a portion of sense amplifier circuitry for dynamic random access memory circuitry and has a lower threshold voltage V_{tl}.

40. (Previously presented) The transistor assembly of claim 34, wherein some of the individual transistors are joined together in a parallel configuration.

Claims 41-43 (Canceled).

Claims 44-50 (Canceled).

51. (Previously presented) The transistor assembly of claim 34, wherein the gate lines are disposed in a direction over the plurality of the active areas, and wherein the widths of the active areas are defined along the direction.

Claims 52-54 (Canceled).

55. (Previously presented) The transistor assembly of claim 34, wherein the widths of the plurality of the active areas are less than one micron.

Claims 56-57 (Canceled).

58. (Previously presented) The transistor assembly of claim 34, wherein the individual transistors comprise an electrically parallel circuit configuration.

Claim 59 (Canceled).

60. (Previously presented) The transistor assembly of claim 34, wherein the gate lines comprise a separate and distinct gate line for each of the plurality of the active areas.

Claims 61-62 (Canceled).